1. **Title of the module**

EENG5680 (EL568) Digital Implementation

1. **School or partner institution which will be responsible for management of the module**

Engineering and Digital Arts

1. **The level of the module (Level 4, Level 5, Level 6 or Level 7)**

Level 5

1. **The number of credits and the ECTS value which the module represents**

15 credits (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn and Spring

1. **Prerequisite and co-requisite modules**

Pre-requisite:

EL305 Introduction to Electronics

EL315 Introduction to Digital Systems Design

1. **The programmes of study to which the module contributes**

BEng Computer Systems Engineering

BEng Computer Systems Engineering with a Year in Industry

BEng Electronic and Communications Engineering

BEng Electronic and Communications Engineering with a Year in Industry

MEng in Computer Systems Engineering

MEng in Computer Systems Engineering with a Year in Industry

MEng Electronic and Communications Engineering

MEng Electronic and Communications Engineering with a Year in Industry

1. **The intended subject specific learning outcomes.  
   On successfully completing the module students will be able to:**

1. demonstrate the necessary skills to model digital components using VHDL;

2. demonstrate an understanding of the operation of CMOS Digital ICs and Memories;

3. demonstrate the necessary skills to design Memory Address decoder systems;

4. demonstrate an understanding of the operation and implementation of a modern CPU.

1. **The intended generic learning outcomes.  
   On successfully completing the module students will be able to:**

1) use ICT,

2) apply critical thinking

3) manage time effectively.

1. **A synopsis of the curriculum**

This module provides an overview of modern digital system implementation. It includes an introduction to CMOS circuit design, fabrication technologies, memory technologies, memory interfacing and an introduction to VHDL/Xilinx.

1. **Reading list (Indicative list, current at time of publication. Reading lists will be published annually)**

Core Text

* Rushton, A (2011) VHDL for logic synthesis, Wiley-Blackwell, Oxford

Recommended Reading

* Mark Zwolinksi (2004) Digital System Design with VHDL, Pearson/Prentice Hall Harlow Roth, Charles H., John, Lizy Kurian (c2008) Digital systems design using VHDL. Thomson, London, Toronto, Ontario.
* Digital Design, Mano, Prentice-Hall
* Pucknell, Douglas A., Eshraghian, Kamran (1994) Basic VLSI Design, Prentice-Hall, London, New York
* Kaeslin, Hubert (c2008) Digital integrated circuit design: from VLSI architectures to CMOS fabrication, Cambridge University Press, Cambridge.
* Ayers, JE (c2010) Digital integrated circuits: analysis and design, CRC, Boca Raton, Fla, London.
* Kishore, K. Lal, Prabhakar, V.S.V. (2009) VLSI Design, I K International Publishing House Pvt. Ltd, New Delhi
* Das, Debaprasad (2010) VLSI Design, Oxford University Press, New Delhi
* Baker, JR (2010) CMOS: circuit design, layout, and simulation, Wiley-IEEE Press, Hoboken, NJ.
* Pedroni, Volnei A. (2008) Digital electronics and design with VHDL, Elsevier Science [distributor], Morgan Kaufmann, Oxford, San Francisco, Calif
* Salemi, R (c2009) FPGA simulation: a complete step-by-step guide
* Amos, Doug, Lesea, Austin, Richter, Rene (2011) FPGA-based Prototyping Methodology Manual: Best Practices in Design-for-Prototyping, Synopsys Press.
* Arora, Mohit (2012) The art of hardware architecture: design methods and techniques for digital circuits, Springer, New York.

1. **Learning and teaching methods**

Total contact hours: 58

Private study hours: 92

Total study hours: 150

1. **Assessment methods**
   1. Main assessment methods

* CAD 1 Introduction to VHDL design experiment (18%)
* Introduction to VHDL and Xilinx 2 assessed workshops (8%)
* The Digital System Implementation examples class (6%)
* Memory Interfacing examples class (8%)
* Exam 2 hours (60%)

In order to obtain credit for this module on IET accredited programmes, the coursework mark and the exam mark must each be greater than or equal to 30% as well as achieving the pass mark for the module. This module will only be considered for compensation if the coursework mark and exam mark are each greater than 30%.

13.2 Reassessment methods

Reassessment instrument: like-for-like

1. **Map of module learning outcomes (sections 8 & 9) to learning and teaching methods (section12) and methods of assessment (section 13)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Module learning outcome** | 8.1 | 8.2 | 8.3 | 8.4 | 9.1 | 9.2 | 9.3 |
| **Learning/ teaching method** |  |  |  |  |  |  |  |
| Private Study |  | **x** | **x** | **x** | **x** | **x** | **x** |
| Lectures | **x** |  |  |  |  |  |  |
| Experimental work | **x** |  |  |  | **x** | **x** | **x** |
| Workshops | **x** |  |  |  | **x** | **x** | **x** |
| Example classes | **x** |  | **x** | **x** |  |  |  |
| **Assessment method** |  |  |  |  |  |  |  |
| Workshop assessments | **x** |  |  |  | **x** | **x** | **x** |
| Example classes |  | **x** |  |  |  |  |  |
| Lab experiment | **x** |  |  |  | **x** | **x** | **x** |
| Exam |  | **x** | **x** | **x** |  |  |  |

1. **Inclusive module design**

The School recognises and has embedded the expectations of current equality legislation, by ensuring that the module is as accessible as possible by design. Additional alternative arrangements for students with Inclusive Learning Plans (ILPs)/declared disabilities will be made on an individual basis, in consultation with the relevant policies and support services.

The inclusive practices in the guidance (see Annex B Appendix A) have been considered in order to support all students in the following areas:

a) Accessible resources and curriculum

b) Learning, teaching and assessment methods

1. **Campus(es) or centre(s) where module will be delivered**

Canterbury

1. **Internationalisation**

This course introduces the fundamentals of digital Integrated Circuit (IC) design and its implementation using CMOS technology *and* the design of digital systems using VHDL and reconfigurable devices such as Xilinx FPGAs. CMOS technology is critical to the design of the modern digital devices that we use every day (phones, computers, TVs etc.). The techniques used to develop these devices are internationally recognised. VHDL is an international IEEE standard Hardware Description Language used for the design of digital systems throughout the world.

**FACULTIES SUPPORT OFFICE USE ONLY**

**Revision record – all revisions must be recorded in the grid and full details of the change retained in the appropriate committee records.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Date approved | Major/minor revision | Start date of the delivery of revised version | Section revised | Impacts PLOs (Q6&7 cover sheet) |
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Revised FSO Jan 2018