1. **Title of the module**

EENG8930 (EL893) - Reconfigurable Architectures

1. **School or partner institution which will be responsible for management of the module**

Engineering and Digital Arts

1. **The level of the module (Level 4, Level 5, Level 6 or Level 7)**

Level 7

1. **The number of credits and the ECTS value which the module represents**

15 credits (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn

1. **Prerequisite and co-requisite modules**

None

1. **The programmes of study to which the module contributes**

MSc/PDip in Digital Systems Engineering

MSc/PDip in Advanced Electronic Systems Engineering

MSc/PDip in Digital Systems Engineering (Integrated Circuit Design)

MSc/PDip in Digital Systems Engineering (Communications)

MSc/PDip in Advanced Communications Engineering (option)

MEng Electronics and Communications Engineering (option)

1. **The intended subject specific learning outcomes.  
   On successfully completing the module students will be able to:**

8.1 Systematically and comprehensively understand reconfigurable architectures including CPLD, FPGA and coarse-grained devices.

8.2 Design, model and verify digital systems using VHDL/Verilog and vendor specific logic synthesis tools and devices.

8.3 Demonstrate critical appraisal in the implementation, testing and debugging of complex digital designs on hardware.

8.4 Comprehensively understand modern heterogeneous Programmable Systems on Chip (PSOC) architectures and devices.

1. **The intended generic learning outcomes.  
   On successfully completing the module students will be able to:**

Use ICT, and will develop core key skills, such as learning effectively, critical thinking and time management. These outcomes are related to the program learning outcomes in the appropriate curriculum maps for the MSc in Embedded Systems and Instrumentation, the MSc/PDip in Wireless Communications and Signal Processing and the MSc/PDip in Advanced Electronic Systems Engineering:

9.1. Students will show an ability to deal with complex issues systematically and creatively and make judgements in the absence of complete data, and show that they are capable of self-direction and problem solving.

9.2. The ability to use and understand a range of modern CAD tools and general ICT.

9.3. Demonstrate the ability to communicate complex ideas and concepts to specialist and non-specialist audiences.

9.4. Show that they are capable of learning independently, use critical thinking and analysis and demonstrate autonomy in time and resource management.

1. **A synopsis of the curriculum**

An Introduction to reconfigurable systems. PLDs, PLAs, FPGAs. Fine grain architectures, Coarse grain architectures, Heterogeneous device Architectures. Case studies. Configuration of FPGA's. Run-time configuration, partial configuration, dynamic reconfiguration. Partitioning systems onto a reconfigurable fabric. Synthesis tools. Timing issues. Verification and Test strategies.

An introduction to Hardware Description Languages. VHDL will be used to illustrate a typical HDL (but this may change to or include Verilog in future). The lectures will define the architectural aspects of a VHDL: entity, architecture, process, package, types, operators, libraries, hierarchy, test benches and synthesisable VHDL. Workshops and laboratories will be used to illustrate how VHDL code is synthesised on to physical hardware devices and a number of challenging practical design examples will be used to illustrate the process.

Basic computer arithmetic and its implementation on reconfigurable logic architectures. Fixed-point and Floating point number representations. The IEEE-754 FP standard. Redundant Number Systems. Residue Number Systems. Methods for Addition and Subtraction. Fast adder architectures. Multi-operand addition. Multiplication: Multiplier architectures; Constant coefficient multipliers; Distributed arithmetic; LUT methods. Special methods: division, square root, the CORDIC algorithm. High-throughput arithmetic. Low-power arithmetic.

1. **Reading list (Indicative list, current at time of publication. Reading lists will be published annually)**

* Arora, Mohit, 2012. The Art of Hardware Architecture: Design Methods and Techniques for Digital Circuits. New York, NY: Springer. ISBN 1461403979
* Ashenden, Peter J. and Dawsonera, The Designer’s Guide to VHDL. Amsterdam: Morgan Kaufmann. ISBN 0080568858
* Athanas, Peter, Pnevmatikatos, Dionisios and Sklavos, Nicolas, 2012. Embedded Systems Design with FPGAs. New York, NY: Springer. ISBN 9781461413615
* Chu, Pong P. and Myilibrary, 2008. FPGA Prototyping by VHDL Examples: Xilinx Spartan-3 version. Hoboken, N.J.: Wiley-Interscience. ISBN 0470185317
* Hamblen, James O., Hall, Tyson S. and Furman, Michael D., Rapid Prototyping of Digital Systems. New York: Springer. ISBN 9780387726700
* Harris, David Money and Harris, Sarah L., 2012. Digital Design and Computer Architecture. San Francisco, Calif: Morgan Kaufmann. ISBN 9780123944245
* Kilts, Steve, 2007. Advanced FPGA Design: Architecture, Implementation, and Optimization. Hoboken, N.J.: Wiley-Interscience. ISBN 9780470127889
* Parhami, Behrooz, 2010. Computer Arithmetic: Algorithms and Hardware Designs. New York: Oxford University Press. ISBN 0195328485
* Pedroni, Volnei A., 2008. Digital Electronics and Design with VHDL. Oxford: Elsevier Science [distributor]. ISBN 0080557554
* Roth, Charles H. and John, Lizy Kurian, c2008. Digital Systems Design using VHDL. London: Thomson. ISBN 9780495244707
* Rushton, Andrew, c2011. VHDL for Logic Synthesis. Oxford: Wiley-Blackwell. ISBN 9780470688472
* Sadrozinski, H. F.-W. and Wu, Jinyuan, 2010. Applications of Field-Programmable Gate Arrays in Scientific Research. London: Taylor & Francis. ISBN 9781439841341
* Salemi, Ray, c2009. FPGA Simulation: A Complete Step-by-step Guide. [S.l:s.n.]. ISBN 9780974164908
* Samanta, Swagata, Design & Implementation of Digital Image Processing using FPGA: FPGA-Based Digital Image Processing. S.l.: LAP Lambert Academic Publishing. ISBN 9783846542729
* Sass, Ronald and Schmidt, Andrew G., Embedded Systems Design with Platform FPGAs: Principles and Practices. Amsterdam: Morgan Kaufmann. ISBN 0123743338

1. **Learning and teaching methods**

Total contact hours: 66

Private study hours: 84

Total study hours: 150

1. **Assessment methods**
   1. Main assessment methods

Assignment (12%)

Assignment (18%)

Examination (70%)

In order to obtain credit for this module on IET accredited programmes, the coursework mark and the exam mark must each be greater than or equal to 40% as well as achieving the pass mark for the module. This module will only be considered for compensation if the coursework mark and exam mark are each greater than 40%.

13.2 Reassessment methods

Like-for-like

1. **Map of module learning outcomes (sections 8 & 9) to learning and teaching methods (section12) and methods of assessment (section 13)**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Module learning outcome** | *8.1* | *8.2* | *8.3* | *8.4* | *9.1* | *9.2* | *9.3* | *9.4* |  |  |  |  |
| **Learning/ teaching method** |  |  |  |  |  |  |  |  |  |  |  |  |
| **Private Study** |  |  |  |  |  |  |  |  |  |  |  |  |
| *Lectures* | **X** |  |  | **X** |  |  |  | **X** |  |  |  |  |
| *Workshops* |  | **X** | **X** |  | **X** | **X** | **X** | **X** |  |  |  |  |
| *Laboratories* |  | **X** | **X** |  | **X** | **X** | **X** | **X** |  |  |  |  |
| **Assessment method** |  |  |  |  |  |  |  |  |  |  |  |  |
| *Workshops* |  | **X** | **X** |  | **X** | **X** | **X** | **X** |  |  |  |  |
| *Laboratories* |  | **X** | **X** |  | **X** | **X** | **X** | **X** |  |  |  |  |
| *Examination* | **X** |  |  | **X** | **X** |  | **X** | **X** |  |  |  |  |

1. **Inclusive module design**

The School recognises and has embedded the expectations of current equality legislation, by ensuring that the module is as accessible as possible by design. Additional alternative arrangements for students with Inclusive Learning Plans (ILPs)/declared disabilities will be made on an individual basis, in consultation with the relevant policies and support services.

The inclusive practices in the guidance (see Annex B Appendix A) have been considered in order to support all students in the following areas:

a) Accessible resources and curriculum

b) Learning, teaching and assessment methods

1. **Campus(es) or centre(s) where module will be delivered**

Canterbury

1. **Internationalisation**

A number of internationally recognised hardware and software tools (e,g, Modelsim, Xilinx, Altera , VHDL) are used to illustrate the material presented in this course and are used throughout the practical exercises. The course also introduces international standards such as the IEEE 754 floating-point arithmetic standards.

**FACULTIES SUPPORT OFFICE USE ONLY**

**Revision record – all revisions must be recorded in the grid and full details of the change retained in the appropriate committee records.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Date approved | Major/minor revision | Start date of the delivery of revised version | Section revised | Impacts PLOs (Q6&7 cover sheet) |
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Revised FSO Jan 2018