***Guidance for the Completion of Module Specification Templates***

Confirmation that this version of the module specification has been approved by the School Learning and Teaching Committee:

…………27th September 2015……………………………………….(date)

**MODULE SPECIFICATION**

1. **Title of the module**

EL673 Digital Systems Design

1. **School or partner institution which will be responsible for management of the module**

Engineering and Digital Arts

1. **Start date of the module**

Revised version start date September 2015

1. **The number of students expected to take the module**

60

1. **Modules to be withdrawn on the introduction of this proposed module and consultation with other relevant Schools and Faculties regarding the withdrawal**

None

1. **The level of the module (e.g. Certificate [C], Intermediate [I], Honours [H] or Postgraduate [M])**

H

1. **The number of credits and the ECTS value which the module represents**

15 (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn and Spring

1. **Prerequisite and co-requisite modules**

EL568 DIGITAL IMPLEMENTATION

1. **The programmes of study to which the module contributes**

BEng Electronic and Communications Engineering

BEng Electronic and Communications Engineering with a Year in Industry

BEng Computer Systems Engineering

BEng Computer Systems Engineering with a Year in Industry

MEng in Electronic and Communications Engineering with a Year in Industry

MEng in Electronic and Communications Engineering

MEng Computer Systems Engineering

MEng Computer Systems Engineering with a Year in Industry

1. **The intended subject specific learning outcomes**

On successful completion of the module, students will:

1. Be able to design reliable digital systems using synchronous design techniques.

2. Be able to design digital systems which are easily testable.

3. Be able to use a range of software tools which synthesize digital systems from VHDL.

4. Understand the major engineering problems associated with building high speed digital systems and how they are solved

These outcomes are related to the learning outcomes in the appropriate curriculum maps as follows:

ECE/ECEwInd: A3, A8-10, B1, B3, B5-6, C1-2, C4-6

CSE/CSEwInd: A3, A8-10, B1, B3, B5-6, C1-2, C4, C6

1. **The intended generic learning outcomes**

On successful completion of the module,

12.1 students will have improved their skills in the use of information and communication technology.

This outcome is related to the learning outcomes in the appropriate curriculum maps as follows: D5,D6, D7.

1. **A synopsis of the curriculum**

Lecture Syllabus

DIGITAL SYSTEM REALISATION

These lectures will: Develop techniques for reliable system design using strictly synchronous design methods. Introduce synthesis tools which map VHDL architecture to FPGAs and consider how to get the best performance from these tools. Review alternative technologies available for implementing digital systems. A practical lab-based assignment will be carried out to gain experience of VHDL design and hardware implementation.

DATA PATH DESIGN

CMOS VLSI revision, Data Path Component building blocks, e.g. Function Blocks, Manchester Carry Chain, ALU, Register Files, Shifters, Structure of Programmable Logic Arrays and their use in the control of the Data Path.

FORMAL TESTABILITY

Testing chips, boards and systems. Single stuck fault models, fault dictionary, test pattern generation.

Testability.

Formal approaches to testability improvement. Scan path techniques.

Boundary scan approach to chip/board testing. IEEE1149.1 Boundary scan - Structure and operation.

Worked Examples.

Coursework

ASSIGNMENT - DIGITAL SYSTEM REALISATION

EXAMPLES CLASS - DATA PATH DESIGN

EXAMPLES CLASS - FORMAL TESTABILITY

1. **Indicative Reading List**

Core Text

Rushton, Andrew (c2011) VHDL for logic synthesis, Wiley-Blackwell, Oxford

Recommended Reading

Ercegovac, Milos D., Lang, Tomás, Moreno, Jaime H (1999) Introduction to digital systems

Roth, Charles H., John, Lizy Kurian (c2008) Digital systems design using VHDL. Thomson, London, Toronto, Ontario

Pedroni, Volnei A. (2008) Digital electronics and design with VHDL, Elsevier Science [distributor], Morgan Kaufmann, Oxford, San Francisco, Calif

Kaeslin, Hubert (c2008) Digital integrated circuit design: from VLSI architectures to CMOS fabrication, Cambridge University Press, Cambridge.

Weste, Neil H. E., Harris, David Money, (c2011) Integrated circuit design, Peason. Boston, Mass, London.

Kishore, K. Lal, Prabhakar, V.S.V. (2009) VLSI Design, I K International Publishing House Pvt. Ltd, New Delhi.

Das, Debaprasad (2010) VLSI design, Oxford University Press, New Delhi

Chandrasetty, Vikram Arkalgud (2011) VLSI design: a practical guide for FPGA and ASIC implementations, Springer, London, New York

Wu, Banqiu, Kumar, Ajay, Ramaswami, Sesh (2011) 3D IC stacking technology, McGraw-Hill Professional, New York.

1. **Learning and Teaching Methods, including the nature and number of contact hours and the total study hours which will be expected of students, and how these relate to achievement of the intended module learning outcomes**

There will be 30 hours of lectures and 2 hours of examples classes. In addition, a VHDL synthesis project is supported by 4 hours of workshops.

Total Contact Hours: 36

Independent Study Hours: 114

Total Study Hours: 150

The lectures and examples classes will address learning outcomes 11.1 to 11.4

The examples classes will address learning outcomes 11.2 and 11.3

The VHDL synthesis project and workshops will address learning outcome 11.3,11.4 and 12.1

1. **Assessment methods and how these relate to testing achievement of the intended module learning outcomes**

The examination:coursework ratio is 60:40. The examination duration is 2 hours

The coursework mark is proportioned as follows:

Digital Systems Realisation VHDL Assignment (70%)

Examples classes (30%)

Learning outcomes 11.1, 11.2, 11.4 and 12.1 are assessed by the examination and coursework. Learning outcomes 11.3, 11.4 and 12.1 are assessed by the VHDL-based assignment.

*In order to obtain credit for this module, the coursework mark and the exam mark must each be greater than or equal to 30% as well as achieving the pass mark for the module.*

*This module will only be considered for compensation if the coursework mark and exam mark are each greater than 30%*

1. **Implications for learning resources, including staff, library, IT and space**

This is a revision of the current EL673 and requires identical resources

1. **The School recognises and has embedded the expectations of current disability equality legislation, and supports students with a declared disability or special educational need in its teaching. Within this module we will make reasonable adjustments wherever necessary, including additional or substitute materials, teaching modes or assessment methods for students who have declared and discussed their learning support needs. Arrangements for students with declared disabilities will be made on an individual basis, in consultation with the University’s disability/dyslexia support service, and specialist support will be provided where needed.**
2. **Campus(es) or Centre(s) where module will be delivered:**

Canterbury