Confirmation that this version of the module specification has been approved by the School Learning and Teaching Committee:

……………27th January 2015…………………………………….(date)

**MODULE SPECIFICATION**

1. **Title of the module**

EL568 Digital Implementation.

1. **School or partner institution which will be responsible for management of the module**

Engineering and Digital Arts

1. **Start date of the module**

**Revised version start date September 2015**

1. **The number of students expected to take the module**

50

1. **Modules to be withdrawn on the introduction of this proposed module and consultation with other relevant Schools and Faculties regarding the withdrawal**

None

1. **The level of the module (e.g. Certificate [C], Intermediate [I], Honours [H] or Postgraduate [M])**

I

1. **The number of credits and the ECTS value which the module represents**

15 (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn and Spring

1. **Prerequisite and co-requisite modules**

EL305 INTRODUCTION TO ELECTRONICS

EL315 INTRODUCTION TO DIGITAL SYSTEMS DESIGN

1. **The programmes of study to which the module contributes**

BEng Computer Systems Engineering

BEng Computer Systems Engineering with a Year in Industry

BEng Electronic and Communications Engineering

BEng Electronic and Communications Engineering with a Year in Industry

MEng in Computer Systems Engineering

MEng in Computer Systems Engineering with a Year in Industry

MEng Electronic and Communications Engineering

MEng Electronic and Communications Engineering with a Year in Industry

1. **The intended subject specific learning outcomes**

On successful completion of the module, students will have:

1. The necessary skills to model digital components using VHDL;

2. An understanding of the operation of CMOS Digital ICs and Memories;

3. Necessary skills to design Memory Address decoder systems;

4. An understanding of the operation and implementation of a modern CPU.

These outcomes are related to the programme learning outcomes in the appropriate curriculum maps as follows:

ECE/ECEwInd: A2,A3,A5,A8,B1,B3-5,C1,C2,C4,C5,C8

CSE/CSEwInd: A2,A3,A5,A8,B1,B3-5,C1,C2,C4,C6,C9

1. **The intended generic learning outcomes**

On successful completion of this module students will be able to

1. use ICT,
2. apply critical thinking
3. manage time effectively.

These outcomes are related to the program learning outcomes in the appropriate curriculum maps as follows:

ECE/ECEwInd: D1,D5,D6,D7

CSE/CSEwInd: D1,D5,D6,D7

1. **A synopsis of the curriculum**

Lecture Syllabus

AN INTRODUCTION TO VHDL

This course introduces the hardware description language, VHDL. A subset of the VHDL language is introduced, which enables moderately complex behavioural and structural models of digital components to be developed. Practical work associated with this course is performed using a Windows-based VHDL compiler and simulator. The Workshops complement the lecture material and provide students with the necessary skills to enable them to use VHDL in their third year projects.

DIGITAL SYSTEM IMPLEMENTATION

Real Logic Gates: voltage and current characteristics, noise immunity and fanout. The MOS

Transistor - detailed operation. Introduction to Stick diagrams.

CMOS Logic Gates. Clocked Logic. Registers, Shift registers.

MEMORY INTERFACING

Structure of Read/Write and Read Only memory cells. Storage mechanisms in Read Only Memories,

Static and Dynamic RAMs. DRAM Cell Design - 3 transistor and 1 transistor, row & column decoders. Memory Read and Write Cycles. Memory Addressing. Multiplexed Addressing. Address decoding, Memory system implementation, Processor-Memory Interfacing. Structure and operation of a small memory system based on RAM devices.

Coursework

EXPERIMENT: (CAD1 Introduction to VHDL Design). 2 days. Assessed.

WORKSHOPS: INTRODUCTION TO VHDL, Six, 2-hour workshops on VHDL/Xilinx, Two of these workshops are assessed.

EXAMPLES CLASS: DIGITAL SYSTEM IMPLEMENTATION

A one-hour examples class. Assessed.

EXAMPLES CLASS: MEMORY INTERFACING

A one-hour examples class. Assessed.

1. **Indicative Reading List**

Core Text

Rushton, A (2011) VHDL for logic synthesis, Wiley-Blackwell, Oxford

Recommended Reading

Mark Zwolinksi (2004) Digital System Design with VHDL, Pearson/Prentice Hall Harlow Roth, Charles H., John, Lizy Kurian (c2008) Digital systems design using VHDL. Thomson, London, Toronto, Ontario.

Digital Design, Mano, Prentice-Hall

Pucknell, Douglas A., Eshraghian, Kamran (1994) Basic VLSI Design, Prentice-Hall, London, New York

Kaeslin, Hubert (c2008) Digital integrated circuit design: from VLSI architectures to CMOS fabrication, Cambridge University Press, Cambridge.

Ayers, JE (c2010) Digital integrated circuits: analysis and design, CRC, Boca Raton, Fla, London.

Kishore, K. Lal, Prabhakar, V.S.V. (2009) VLSI Design, I K International Publishing House Pvt. Ltd, New Delhi

Das, Debaprasad (2010) VLSI Design, Oxford University Press, New Delhi

Baker, JR (2010) CMOS: circuit design, layout, and simulation, Wiley-IEEE Press, Hoboken, NJ.

Pedroni, Volnei A. (2008) Digital electronics and design with VHDL, Elsevier Science [distributor], Morgan Kaufmann, Oxford, San Francisco, Calif

Salemi, R (c2009) FPGA simulation: a complete step-by-step guide

Amos, Doug, Lesea, Austin, Richter, Rene (2011) FPGA-based Prototyping Methodology Manual: Best Practices in Design-for-Prototyping, Synopsys Press.

Arora, Mohit (2012) The art of hardware architecture: design methods and techniques for digital circuits, Springer, New York.

1. **Learning and Teaching Methods, including the nature and number of contact hours and the total study hours which will be expected of students, and how these relate to achievement of the intended module learning outcomes**

There will be 28 hours of lectures, 18 hours of experimental work, 12 hours of workshops and 2 hours of examples classes.

The Introduction to VHDL lecture course and examples class delivers learning outcome 11.1, as do the workshops and experiment.

Learning outcomes 11.2 and 11.4 are delivered through the Digital System Implementation course.

The Memory interfacing course and examples class will deliver learning outcomes 11.3 and 11.4.

Generic learning outcomes 12.1-12.3 are addressed by the experiment and the workshops.

Total Contact Hours: 58

Independent Study Hours: 92

Total Study Hours: 150

1. **Assessment methods and how these relate to testing achievement of the intended module learning outcomes**

Learning outcome 11.1 is assessed through the Laboratory experiment and the Introduction to VHDL and Xilinx workshops. The Digital System Implementation examples class assesses learning outcome 11.2. The examination assesses learning outcomes 11.2, 11.3, 11.4. Weighting between coursework and the examination is 40:60. The examination duration is 2 hours.

The coursework mark is proportioned as follows:

CAD 1 Introduction to VHDL design experiment (45%)

Introduction to VHDL and Xilinx 2 assessed workshops (20%)

The Digital System Implementation examples class (15%)

Memory Interfacing examples class (20%)

The generic learning outcomes 12.1 to 12.3 are assessed by the experiment and workshops.

*In order to obtain credit for this module, the coursework mark and the exam mark must each be greater than or equal to 30% as well as achieving the pass mark for the module.*

*This module will only be considered for compensation if the coursework mark and exam mark are each greater than 30%*

1. **Implications for learning resources, including staff, library, IT and space**

None

1. **The School recognises and has embedded the expectations of current disability equality legislation, and supports students with a declared disability or special educational need in its teaching. Within this module we will make reasonable adjustments wherever necessary, including additional or substitute materials, teaching modes or assessment methods for students who have declared and discussed their learning support needs. Arrangements for students with declared disabilities will be made on an individual basis, in consultation with the University’s disability/dyslexia support service, and specialist support will be provided where needed.**
2. **Campus(es) or Centre(s) where module will be delivered:**

Canterbury