1. **Title of the module**

EENG8940 (EL894) - Digital Integrated Circuit Design

1. **School or partner institution which will be responsible for management of the module**

Engineering and Digital Arts

1. **The level of the module (Level 4, Level 5, Level 6 or Level 7)**

Level 7

1. **The number of credits and the ECTS value which the module represents**

15 credits (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn

1. **Prerequisite and co-requisite modules**

None

1. **The programmes of study to which the module contributes**

MSc/PDip in Advanced Digital Systems Engineering

MSc/PDip in Advanced Digital Systems Engineering (Integrated Circuit Design)

1. **The intended subject specific learning outcomes.
On successfully completing the module students will be able to:**

Have:

1. A detailed understanding of the operation of the MOS transistor and an ability to design digital circuits using CMOS technology that operate within a specified range of voltages, currents and temperatures when fabricated on an integrated circuit. An ability to use CAD tools to model and verify the operation of logic CMOS circuits.

2. A detailed practical understanding of CMOS design rules and the impact of circuit layout on circuit performance. An ability to use CAD tools to build and verify the operation of basic CMOS logic circuits. An appreciation of different circuit design techniques including full- and semi-custom methods and the use of CAD tools and their conflicting impact on device cost and designer productivity.

3. A detailed understanding of basic combinatorial and sequential logic circuits and an appreciation of the impact of different clocking strategies on circuit design and performance.

4. An understanding of CMOS memory design including ROM, PLA, Static and Dynamic RAMs and memory addressing techniques including row & column decoders. An appreciation of other volatile and non-volatile memory types such as EPROM, EEPROM, FRAM and MRAM and their current and future impact on modern fabrication technologies.

5. An understanding of Data Path components including Adders, ALUs, Registers and Multiplier Design. The ability to design, build and verify the operation a simple data-path circuit using modern CAD tools.

6. An appreciation of digital fault mechanisms and formal test strategies for circuits and chips. An understanding of formal methods for Automatic Test Pattern Generation (ATPG). A detailed understanding of the IEEE1149.1 Boundary Scan (or JTAG) Standard and its derivatives.

7. The ability to design and build a digital circuit from a system specification and evaluate its performance.

1. **The intended generic learning outcomes.
On successfully completing the module students will be able to:**

1. Show an ability to deal with complex issues systematically and creatively and make judgements in the absence of complete data, and show that they are capable of self-direction and problem solving.

2. Use and understand a range of modern CAD tools and general ICT.

3. Demonstrate the ability to communicate complex ideas and concepts to specialist and non-specialist audiences.

4. Show that they are capable of learning independently, use critical thinking and analysis and demonstrate autonomy in time and resource management.

1. **A synopsis of the curriculum**

This module will cover the fundamental concepts of digital circuit design using CMOS technology. It begins with an overview of CMOS technology and introduces the simple and extended circuit models for NMOS and CMOS transistor devices. The module will cover transistor level design of logic gates (both combinatorial and sequential) at the device and layout level. It will include memory design (ROM, SRAM and DRAM) and memory decode logic. Static and dynamic clocking methods will be described including examples of 1-phase, 2-phase, 4-phase clocking and Domino and NORA logic techniques. The course will also cover alternative low-power logic families such as DCVS and Adiabatic Logic and discuss the implications of modern methods such as the use near- and sub-threshold logic on circuit design. Chip level design methodologies such as full-custom, semi-custom and standard cell will be explored. The course will use appropriate CAD tools (Cadence®, Synopsys®, Tanner®) and modern fabrication technologies (down to 65 nm) that are common in the design of CMOS integrated circuits to illustrate the range of techniques and methods described in the lectures. Students will use knowledge gained in lectures and workshops to develop their own IC designs in the laboratories.

1. **Reading list (Indicative list, current at time of publication. Reading lists will be published annually)**
* Kang, S. Leblebici, K (1999) CMOS Digital Integrated Circuits: Analysis and Design. WCB/McGraw-Hill. ISBN 0-07-116427-8
* Ayers, J. E. (2010) Digital Integrated Circuits: Analysis and Design, CRC Press ISBN: 978-1-4200-6987-7
* Weste, N. H. H. and Money Harris, D. (2011) Integrated Circuit Design, Pearson ISBN: 978-0-321-69694-6
* Soin, R. S. Maloberti, F. Franca, J. (Ed) (1991) Analogue-Digital ASICs: Circuit Techniques, Design Tools, and Applications. Peter Perigrinus Ltd ISBN: 0-86341-259-9
* Kaeslin, H. (2015) Top-Down Digital VLSI Design: From Architectures to Gate-Level Circuits and FPGAs. Morgan Kaufmann ISBN: 978-0-12-800730-3
* Salman, E. and Friedman, E. G. (2012) High Performance Integrated Circuit Design. McGraw Hill ISBN 978-0-07-163576-9
* Uyemura, J. P. (1999) CMOS Logic Circuit Design. Kluwer. ISBN 0-7923-8452-0
1. **Learning and teaching methods**

Total contact hours: 90

Private study hours: 60

Total study hours: 150

1. **Assessment methods**
	1. Main assessment methods

Coursework (40%)

Examination (60%)

13.2 Reassessment methods

Like-for-like

1. **Map of module learning outcomes (sections 8 & 9) to learning and teaching methods (section12) and methods of assessment (section 13)**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Module learning outcome** | *8.1* | *8.2* | *8.3* | *8.4* | *8.5* | *8.6* | *8.7* | *9.1* | *9.2* | *9.3* | *9.4* |
| **Learning/ teaching method** |  |  |  |  |  |  |  |  |  |  |  |
| *Private Study* |  |  |  |  |  |  |  | **X** |  |  | **X** |
| *Lectures* | **X** | **X** | **X** | **X** | **X** | **X** |  |  |  |  |  |
| *Workshops* | **X** | **X** | **X** | **X** | **X** |  | **X** | **X** | **X** | **X** | **X** |
| *Mini-project* | **X** | **X** | **X** | **X** | **X** |  | **X** | **X** | **X** | **X** | **X** |
| **Assessment method** |  |  |  |  |  |  |  |  |  |  |  |
| *Workshop assessments* | **X** | **X** | **X** | **X** | **X** |  | **X** | **X** | **X** | **X** | **X** |
| *Mini-project* | **X** | **X** | **X** | **X** | **X** |  | **X** | **X** | **X** | **X** | **X** |
| *Examination* | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** |

1. **Inclusive module design**

The School recognises and has embedded the expectations of current equality legislation, by ensuring that the module is as accessible as possible by design. Additional alternative arrangements for students with Inclusive Learning Plans (ILPs)/declared disabilities will be made on an individual basis, in consultation with the relevant policies and support services.

The inclusive practices in the guidance (see Annex B Appendix A) have been considered in order to support all students in the following areas:

a) Accessible resources and curriculum

b) Learning, teaching and assessment methods

1. **Campus(es) or centre(s) where module will be delivered**

Canterbury

1. **Internationalisation**

The module makes comprehensive use of internationally recognised IC development tools from Cadence and Mentor Graphics (soon to be part of Siemens) to illustrate the design of digital integrated circuits. Design rules are used from internationally recognised fabrication foundries such as TSMC, UMC and Austria Mikro Systems to illustrate the current state of the art in IC technology.

**FACULTIES SUPPORT OFFICE USE ONLY**

**Revision record – all revisions must be recorded in the grid and full details of the change retained in the appropriate committee records.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Date approved | Major/minor revision | Start date of the delivery of revised version | Section revised | Impacts PLOs (Q6&7 cover sheet) |
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Revised FSO Jan 2018