1. **Title of the module**

EENG6730 (EL673) Digital Systems Design

1. **Division or partner institution which will be responsible for management of the module**

Computing, Engineering and Mathematical Sciences

1. **The level of the module (Level 4, Level 5, Level 6 or Level 7)**

Level 6

1. **The number of credits and the ECTS value which the module represents**

15 credits (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn and Spring

1. **Prerequisite and co-requisite modules**
2. **The programmes of study to which the module contributes**

BEng Electronic and Communications Engineering

BEng Electronic and Communications Engineering with a Year in Industry

BEng Computer Systems Engineering

BEng Computer Systems Engineering with a Year in Industry

MEng in Electronic and Communications Engineering with a Year in Industry

MEng in Electronic and Communications Engineering

MEng Computer Systems Engineering

MEng Computer Systems Engineering with a Year in Industry

BEng Electronic and Communications Engineering

BEng Electronic and Communications Engineering with a Year in Industry

BEng/MEng Electronic and Computer Engineering

BEng /Meng Electronic and Computer Engineering with a Year in Industry

1. **The intended subject specific learning outcomes.  
   On successfully completing the module students will be able to:**

1. Design reliable digital systems using synchronous design techniques.

2. Design digital systems which are easily testable.

3. Appreciate a range of software for synthesis of digital systems.

4. Understand the major engineering problems associated with building high speed digital systems and how they are solved

1. **The intended generic learning outcomes.  
   On successfully completing the module students will be able to:**

1. Manage their own learning including through the use of ICT.

1. **A synopsis of the curriculum**

This module looks at the methodology of designing and implementing large digital systems. Students taking this module will learn how to design reliable digital systems using synchronous design techniques, will learn how to design digital systems which are easily testable and will be able to use a range of software tools to synthesize digital systems.

1. **Reading list (Indicative list, current at time of publication. Reading lists will be published annually)**

Core Text

* Rushton, Andrew (c2011) VHDL for logic synthesis, Wiley-Blackwell, Oxford

Recommended Reading

* Ercegovac, Milos D., Lang, Tomás, Moreno, Jaime H (1999) Introduction to digital systems
* Roth, Charles H., John, Lizy Kurian (c2008) Digital systems design using VHDL. Thomson, London, Toronto, Ontario
* Pedroni, Volnei A. (2008) Digital electronics and design with VHDL, Elsevier Science [distributor], Morgan Kaufmann, Oxford, San Francisco, Calif
* Kaeslin, Hubert (c2008) Digital integrated circuit design: from VLSI architectures to CMOS fabrication, Cambridge University Press, Cambridge.
* Weste, Neil H. E., Harris, David Money, (c2011) Integrated circuit design, Peason. Boston, Mass, London.
* Kishore, K. Lal, Prabhakar, V.S.V. (2009) VLSI Design, I K International Publishing House Pvt. Ltd, New Delhi.
* Das, Debaprasad (2010) VLSI design, Oxford University Press, New Delhi
* Chandrasetty, Vikram Arkalgud (2011) VLSI design: a practical guide for FPGA and ASIC implementations, Springer, London, New York
* Wu, Banqiu, Kumar, Ajay, Ramaswami, Sesh (2011) 3D IC stacking technology, McGraw-Hill Professional, New York.

1. **Learning and teaching methods**

Total contact hours: 36

Private study hours: 114

Total study hours: 150

1. **Assessment methods**
   1. Main assessment methods

* Digital Systems Realisation software Assignment (28%)
* Examples class assignment (12%)
* Exam 2 hours (60%)

13.2 Reassessment methods

like-for-like

1. **Map of module learning outcomes (sections 8 & 9) to learning and teaching methods (section12) and methods of assessment (section 13)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Module learning outcome** | 8.1 | 8.2 | 8.3 | 8.4 | 9.1 |
| **Learning/ teaching method** |  |  |  |  |  |
| Private Study | **x** | **x** | **x** | **x** | **x** |
| Lectures | **x** | **x** | **x** | **x** |  |
| Example classes |  | **x** | **x** |  |  |
| Workshops |  |  | **x** | **x** | **x** |
| **Assessment method** |  |  |  |  |  |
| Digital Systems Realisation Assignment |  |  | **x** | **x** | **x** |
| Examples class assignment | **x** | **x** |  | **x** | **x** |
| Exam | **x** | **x** | **x** | **x** | **X** |

1. **Inclusive module design**

The Division recognises and has embedded the expectations of current equality legislation, by ensuring that the module is as accessible as possible by design. Additional alternative arrangements for students with Inclusive Learning Plans (ILPs)/declared disabilities will be made on an individual basis, in consultation with the relevant policies and support services.

The inclusive practices in the guidance (see Annex B Appendix A) have been considered in order to support all students in the following areas:

a) Accessible resources and curriculum

b) Learning, teaching and assessment methods

1. **Campus(es) or centre(s) where module will be delivered**

Canterbury

1. **Internationalisation**

The design and implementation of digital systems using modern hardware techniques and technologies is of international importance. Many aspects of our modern world rely on complex but reliable digital hardware which is constantly evolving as the technology continues to develop at a rapid pace. Consider just how many times a day we interact with a digital system and how modern digital communication technologies enables the work we do to be broadcast and disseminated to an international audience. An understanding of this core technology and the methods for designing such systems is essential to many engineering and design industries and services.

**DIVISIONAL USE ONLY**

**Revision record – all revisions must be recorded in the grid and full details of the change retained in the appropriate committee records.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Date approved | Major/minor revision | Start date of the delivery of revised version | Section revised | Impacts PLOs (Q6&7 cover sheet) |
| 15/10/2020 | Minor | Sept 2021/22 | 6, 7, 8, 9, 10, 13, 14 | NO |
|  |  |  |  |  |