**Title of the module**

EENG5680 (EL568) Digital Implementation

1. **Division or partner institution which will be responsible for management of the module**

Computing, Engineering and Mathematical Sciences

1. **The level of the module (Level 4, Level 5, Level 6 or Level 7)**

Level 5

1. **The number of credits and the ECTS value which the module represents**

15 credits (7.5 ECTS)

1. **Which term(s) the module is to be taught in (or other teaching pattern)**

Autumn and Spring

1. **Prerequisite and co-requisite modules**

 None

1. **The courses to which the module contributes**

BEng Computer Systems Engineering

BEng Computer Systems Engineering with a Year in Industry

BEng Electronic and Communications Engineering

BEng Electronic and Communications Engineering with a Year in Industry

MEng in Computer Systems Engineering

MEng in Computer Systems Engineering with a Year in Industry

MEng Electronic and Communications Engineering

MEng Electronic and Communications Engineering with a Year in Industry

BEng Electronic and Computer Engineering with a Foundation Year

BEng/MEng Electronic and Computer Engineering

BEng/MEng Electronic and Computer Engineering with a Year in Industry

1. **The intended subject specific learning outcomes.
On successfully completing the module students will be able to:**

1. demonstrate the necessary skills to model digital components using VHDL;

2. demonstrate an understanding of the operation of CMOS Digital ICs and Memories;

3. demonstrate the necessary skills to design Memory Address decoder systems;

4. demonstrate an understanding of the operation and implementation of a modern CPU.

1. **The intended generic learning outcomes.
On successfully completing the module students will be able to:**

1) demonstrate ICT skills necessary for employment

2) show critical knowledge of methods of enquiry;

3) manage time effectively.

1. **A synopsis of the curriculum**

This module provides an overview of modern digital system implementation. It includes an introduction to CMOS circuit design, fabrication technologies, memory technologies, memory interfacing and an introduction to VHDL/Xilinx.

1. **Reading list (Indicative list, current at time of publication. Reading lists will be published annually)**

Recommended Reading:

* Rushton, A (2011) VHDL for logic synthesis, Wiley-Blackwell, Oxford
* Neaman, Donald (2010) Microelectronics: Circuit Analysis and Design, Fourth Edition. McGrawHill.
* Bogart, Theodore F.; Beasley, Jeffrey S.; Rico, Guillermo (2004) Electronic Devices and Circuits, Pearson/Prentice Hall. ISBN. 9780131111424.
* Jain, R. P. (2003) Modern Digital Electronics. McGrawHill.
1. **Learning and teaching methods**

Total contact hours: 38

Private study hours: 112

Total study hours: 150

1. **Assessment methods**
	1. Main assessment methods
* Homework 1 (5%)
* Homework 2 (5%)
* VHDL Workshop 1 (12%)
* VHDL Workshop 2 (18%)
* Exam, 2 hours (60%)

13.2 Reassessment methods

like-for-like

1. **Map of module learning outcomes (sections 8 & 9) to learning and teaching methods (section12) and methods of assessment (section 13)**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Module learning outcome** | 8.1 | 8.2 | 8.3 | 8.4 | 9.1 | 9.2 | 9.3 |
| **Learning/ teaching method** |  |  |  |  |  |  |  |
| Private Study | **x** | **x** | **x** | **x** | **x** | **x** | **x** |
| Lectures  | **x** | **x** | **x** | **x** |  |  |  |
| VHDL Workshops  | **x** |  |  | **x** | **x** | **x** | **x** |
| **Assessment method** |  |  |  |  |  |  |  |
| Workshop assessments | **x** |  |  | **x** | **x** | **x** | **x** |
| Homeworks |  | **x** | **x** | **x** |  |  |  |
| Exam |  | **x** | **x** | **x** |  |  |  |

1. **Inclusive module design**

The Division recognises and has embedded the expectations of current equality legislation, by ensuring that the module is as accessible as possible by design. Additional alternative arrangements for students with Inclusive Learning Plans (ILPs)/declared disabilities will be made on an individual basis, in consultation with the relevant policies and support services.

The inclusive practices in the guidance (see Annex B Appendix A) have been considered in order to support all students in the following areas:

a) Accessible resources and curriculum

b) Learning, teaching and assessment methods

1. **Campus(es) or centre(s) where module will be delivered**

Canterbury

1. **Internationalisation**

Engineering is an international discipline with techniques developed and refined by scientists across the globe. Mastery of the subject-specific learning outcomes, will equip students to apply the theories and techniques of this module in a wide range of international contexts. This course introduces the fundamentals of digital Integrated Circuit (IC) design and its implementation using CMOS technology *and* the design of digital systems using VHDL and reconfigurable devices such as Xilinx FPGAs. CMOS technology is critical to the design of the modern digital devices that we use every day (phones, computers, TVs etc.). The techniques used to develop these devices are internationally recognised. VHDL is an international IEEE standard Hardware Description Language used for the design of digital systems throughout the world. The module team includes many members of staff with international experience of teaching and research collaboration. In compiling the reading list, consideration has been given to the range of texts that are available internationally and a selection of texts has been identified to complement the delivery of the material. The support provided to the students is also internationally attuned given our international student body.

**DIVISION USE ONLY**

**Revision record – all revisions must be recorded in the grid and full details of the change retained in the appropriate committee records.**

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| Date approved | Major/minor revision | Start date of the delivery of revised version | Section revised | Impacts PLOs (Q6&7 cover sheet) |
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